REMARKS

Reconsideration of this application, as amended, is respectfully requested.

Claims 12-17 and 23-36 are pending. Claims 12-17 and 23-36 stand rejected.

Claims 12, 23, and 30 have been amended. No claims have been canceled. No claims have been added. Support for the amendments is found in the specification, the drawings, and in the claims as originally filed. Applicant submits that the amendments do not add new matter.

Applicant reserves all rights with respect to the applicability of the Doctrine of Equivalents.

INTERVIEW SUMMARY

The applicant's amendments presented in the response to the Office Action mailed on May 10, 2007 were discussed in light of the cited reference. Applicant explained the claimed invention to the Examiner. The Examiner asked applicant to provide a supplemental amendment in light of the discussion. No formal agreement was reached as to any claims.

REJECTIONS UNDER 35 U.S.C. § 102

Claims 12-17 and 23-36 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,765,258 of Wu et al. ("Wu").

Applicant respectfully submit that amended claim 12 is not anticipated by Wu under 35 U.S.C. § 102(e).

Applicant has amended claim 12 to read as follows:

> A flash memory cell comprising:
>
> a plurality of gate stacks formed on a substrate, and a plurality of active regions formed in the substrate, wherein each of the plurality of the gate stacks has a gate stack length and a gate stack width;
>
> an interlayer dielectric (ILD) deposited over the gate stacks and the active regions;
>
> a single continuous one-dimensional slot patterned in the ILD that exposes the plurality of the gate stacks, wherein the one dimensional slot is to provide

access to the plurality of active regions to form a bit line to contact the plurality of active regions through the single continuous one-dimensional slot, wherein the single continuous one-dimensional slot has a length along the length of the bit line that is substantially larger than a width that is the gate stack width.

(Amended claim 12) (emphasis added)

Wu discloses stack-gate flash memory cell structure and its contactless flash memory arrays. More specifically, Wu a plurality of common source conductive bit lines and a plurality of common-drain conductive islands being integrated with a plurality of bit lines (Abstract). In particular, Wu discloses

> FIG. 3I(b) shows that a planarized capping-oxide layer 315a is formed over each of the composite control-gate conductive layers 314b, and a metal layer 316 is then formed over the formed structure and is patterned by the masking step as described in FIG. 3I(a); and the metal layer 316 and the planarized second conductive layers 309a are simultaneously etched to form a plurality of metal bit-lines 316a integrated with a plurality of planarized second conductive islands 309c for forming a contactless NOR-type flash memory array of the present invention. It should be noted that the intergate-dielectric layer 313 over the planarized thick-oxide layers 310a and the planarized second conductive layers 309a are removed by the CMP process and the thin thermal poly-oxide layer over each of the planarized second conductive layers 309a is also removed. The exposed planarized second conductive layer 309a is preferably silicided to form a refractory-metal silicide layer before forming the metal layer 316. Similarly, the metal layer 316 may comprise an aluminum or copper layer being formed on a barrier-metal layer such a titanium-nitride (TiN) or tantalum-nitride (TaN) layer.

(Wu, col. 8, lines 26-48) (emphasis added)

Further, Wu discloses

> FIG. 4 shows a top plan view of the contactless parallel common-source/drain conductive bit-line flash memory array, in which a cross-sectional view along a A-A' line is shown in FIG. 3I(a). From FIG. 4, it is clearly seen that the plurality of common-source conductive bit-lines (CSBL's) and the plurality of common-drain conductive bit-lines (CDBL's) are formed in parallel and transversely to the plurality of parallel STI regions; and the plurality of metal word-lines (WL's) integrated with the plurality of planarized control-gate conductive islands 314b are formed transversely to the plurality of common-source/drain conductive bit-lines (CSBL's/CDBL's).
>
> (Wu, col. 8, lines 44-60) (emphasis added)

Thus, Wu merely discloses that the planarized capping-oxide layer is formed over each of the composite control-gate conductive layers. In contrast, amended claim 12 refers to a single continuous one-dimensional slot patterned in the ILD that exposes the plurality of the gate stacks, wherein the one dimensional slot is to provide access to the plurality of active regions to form a bit line to contact the plurality of active regions through the single continuous one-dimensional slot, wherein the single continuous one-dimensional slot has a length along the length of the bit line that is substantially larger than a width that is the gate stack width.

Because Wu fails to disclose all limitations of amended claim 12, applicant respectfully submits that amended claim 12 is not anticipated by Wu under 35 U.S.C. § 102(e).

With respect to amended independent claim 23, Wu merely discloses the planarized capping-oxide layer that is formed over each of the composite control-gate conductive layers, and the conductive bit-lines that are formed in parallel and transversely to the plurality of parallel STI regions (col. 8, lines 26-48). In contrast, amended claim 23 refers to a single continuous one-dimensional slot patterned in the ILD that exposes the plurality of the gate stacks providing access to the plurality of active regions; and a bit line formed in the single continuous one-dimensional slot, the bit line in contact with the top surface of the gate stacks and in contact with the plurality of active regions, wherein the single continuous one-dimensional slot has a length along the length of the bit line that is substantially larger than a width that is a gate stack width .

Because Wu fails to disclose all limitations of amended independent claim 23, applicant respectfully submits that amended claim 23 is not anticipated by Wu under 35 U.S.C. § 102(e).

Given that amended independent claim 30 contains at least the limitations similar to those discussed with respect to amended claim 23, applicant respectfully submits that claim 30 is not anticipated by Wu under 35 U.S.C. § 102(e).

Given that claims 13-17, 24-29, and 31-36 depend from amended independent claims 12, 23, and 30 respectively, and add additional limitations, applicant respectfully submits that claims 13-17, 24-29, and 31-36 are not anticipated by Wu under 35 U.S.C. § 102(e).

It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections and objections have been overcome. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call Tatiana Rossin at (408) 720-8300.

If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

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